REMARKS/ARGUMENTS

Claims 1-20 are pending herein. Claim 8 has been rewritten in independent form. Applicants respectfully submit that no new matter has been added.

1. Examiner Ha is thanked for courtesies extended to Applicants' representative (Nicole Buckner) during a telephonic interview on November 1, 2004. Examiner Ha tentatively agreed with the arguments discussed during the telephonic interview, and invited Applicants to submit the arguments in a written response.

2. Applicants appreciate Examiner Ha indicating that claims 16-20 are allowed, and that claim 8 would be allowed if rewritten in independent form. Claim 8 has been so rewritten. In addition to claims 8 and 16-20, Applicants respectfully submit that all claims pending herein are in condition for allowance for the reasons explained below, and respectfully request that the PTO issue a Notice of Allowance for this application in due course.

3. Claims 1-7 and 9-15 were rejected under §103(a) over Naito in view of Dohya. Applicants respectfully traverse this rejection.

Independent claim 1 recites an intermediate laminated structure including, among other things, a plurality of unfired ceramic plates, and at least a first hole in one of the plurality of unfired ceramic plates that has the same shape and cross-sectional area as respective first holes in the remaining plurality of unfired ceramic plates such that the first holes define a cylinder of constant cross-sectional area throughout the entire thickness of the intermediate laminated structure.

Independent claim 11 recites an intermediate laminated circuit substrate including, among other things, a plurality of insulators comprising unfired ceramic plates, a plurality of conductors formed on the insulators, and at least one cylinder defined by a plurality of first holes formed in each of the plurality of insulators and conductors by a punching operation and passing through all of the insulators and conductors, wherein at least a first hole in one of the plurality of insulators and

conductors has the same shape and cross-sectional area as respective first holes in the remaining plurality of insulators and conductors such that the cylinder has a constant cross-sectional area throughout the entire thickness of the intermediate laminated circuit substrate.

In the Office Action, Examiner Ha asserted that Naito discloses "a multi-layer capacitor/intermediate laminated structure comprising: a plurality of unfired ceramic plates/ceramic green sheets 32 stacked along a laminating direction (figure 2a), each of said plates having a plurality of holes (38 & 39) formed therethrough, wherein at least a first hole in one of said plurality of unfired ceramic plates has the same shape and cross-sectional area as respective first holes in the remaining plurality of unfired ceramic plates (figure 1) such that said first holes define the cylinder of constant cross-sectional area throughout the entire thickness of said intermediate laminated structure (figure 2a)" (Office Action, page 2, line 20--page 3, line 2). Applicants respectfully disagree with Examiner Ha's characterization of Naito.

For example, Applicants respectfully submit that reference numerals 38 and 39 in Naito's Fig. 1 do not correspond to a plurality of holes, as Examiner Ha asserted, but instead represent the external electrodes that are formed on the outer surface 37 of the capacitor body 35 and that are connected to the connection portions 40 and 41, respectively, to ensure counter-current flow in the connection portions 40, 41 (see Naito, Col. 5, lines 43-46). Moreover, in Naito's Fig. 1, the diameters of the circles 38, 39 representing the external electrodes on the outer surface 37 of the capacitor body 35 do not correspond to the diameter of the holes that are actually formed in Naito's ceramic green sheets and electrode layers, as clearly shown in Naito's Fig. 2A.

Although Naito discloses that holes are formed in the dielectric layers 32, and the final (baked) structure in Naito's Fig. 2A shows that holes are also provided in the internal electrode layers 33 and 34, Applicants respectfully submit that the respective holes formed in the various layers of Naito's final (baked) multi-layer capacitor do not define a cylinder having a constant cross-sectional area throughout the entire thickness of the multi-layer capacitor, as claimed.

That is, in the multi-layer capacitor shown in Naito's Fig. 2A, the final (baked) structure includes a plurality of dielectric layers 32 that are alternately laminated with internal electrodes 33, 34. Connection portions 41 connect internal electrodes 34 and pass through the wider openings 42 in the internal electrodes 33 such that connection portions 41 are insulated from the internal electrodes 33. It can be seen from Naito's Fig. 2A that the wider openings 42 formed in the electrodes 33 are larger than the holes formed in the internal electrodes 34 and the dielectric layers 32 through which the connection portion 41 pass in order to insulate the connection portions 41 from the electrodes 33. Similarly, connection portions 40 connect internal electrodes 33 and pass through the wider openings 43 in the electrodes 34 such that the connection portions 40 are electrically insulated from the internal electrodes 34. Again, it is clear from Naito's Fig. 2A that the wider openings 43 formed in electrodes 34 are larger than the holes formed in the internal electrodes 33 and the dielectric layers 34 through which the connection portions 40 pass for the same insulation purposes described above. Since the respective diameters of the openings 42 and 43 formed in the internal electrodes 33 and 34 are greater than the respective diameters of the other openings formed in the electrodes 33 and 34, and are greater than the diameter of the respective openings formed in the dielectric layers 32, Applicants respectfully submit that it is clear that the path of the respective openings throughout the entire thickness of the final multi-layer structure shown in Naito's Fig. 2A does not define a cylinder of constant cross-sectional area throughout the entire thickness of the structure, as claimed.

Further, independent claims 1 and 11 respectively recite an *intermediate* laminated structure and an intermediate laminated circuit substrate, not a final (baked) structure, as shown in Naito's Fig. 2A. Applicants respectfully submit, however, that Naito does not disclose or suggest any intermediate laminate that would meet the claimed limitations. For example, Naito's internal electrodes 33, 34 are formed on the green sheets 32, which are then laminated as described in Col. 5, lines 25-39 of Naito. Prior to that lamination, however, the connection portions 40 and 41 are formed, "for example, by forming holes in the ceramic green sheets before they are laminated

together and filling the holes with conductive paste before they are stacked one on top of the other" (Naito, Col. 5, lines 63-67). There is no disclosure, however, of how those holes are formed, of how the corresponding openings and wider insulating openings in the internal electrodes are formed, of how the respective holes are aligned prior to or during lamination, or if any steps are taken to align the holes at all. In fact, Applicants respectfully submit that the laminated ceramic green sheets in an intermediate stage of forming Naito's multi-layer structure do not even include holes as claimed, since the holes formed in the ceramic green sheets are filled with conductive paste prior to lamination, as mentioned above.

Even if, *arguendo*, the PTO were to argue that the holes in the green sheets still exist, though filled with conductive paste, in an intermediate stage of Naito's laminated structure, Applicants respectfully submit that the cross-sectional area of the path of the paste-filled holes in the ceramic green sheets is not constant, and in fact, is interrupted by the different sizes of the holes (openings) formed in the respective intervening internal electrodes 33, 34 throughout the entire thickness of the structure. In that manner, even Naito's intermediate laminated structure does not include any structures that would define a cylinder having a constant cross-sectional area throughout the entire thickness of the intermediate laminated structure, as claimed.

Examiner Ha admitted that Naito does not disclose that the holes are formed by punching, and applied Dohya in an attempt to overcome the admitted deficiency of Naito. Applicants respectfully submit, however, that Dohya does not overcome the above-mentioned deficiencies of Naito by merely disclosing that holes can be formed in ceramic green sheets by punching. Furthermore, Applicants respectfully submit there is no disclosure or suggestion in Dohya with respect to punching holes in other layers, such as Naito's electrode layers, which, according to Naito, are formed on the green sheets prior to forming the holes and laminating the layers, as explained above. Accordingly, Applicants respectfully submit that one of ordinary skill in the are would not have been motivated to form the holes in Naito's green ceramic sheet layers having the electrode layers formed thereon by punching based merely on the disclosure of Dohya, as Examiner Ha suggested.

With respect to dependent claim 7, Examiner Ha asserted that Naito discloses "unfired ceramic plates/dielectric ceramics comprising ceramic material (column 5, lines 26-28)" (Office Action, page 4, lines 19-20). Applicants respectfully submit, however, that the cited portion of Naito merely discloses that the capacitor main body includes a plurality of dielectric material layers preferably made of a ceramic dielectric material. That is, there is simply no disclosure or suggestion in Naito that the unfired ceramic plates comprise a compound insulating material comprising a plastic resin and a ceramic material, as recited in dependent claim 7.

Independent claims 9 and 15 are product-by-process claims. Independent claim 9 is a product-by-process claim for an intermediate laminated structure including, among other things, at least a first hole in one of a plurality of unfired ceramic plates that has the same shape and cross-sectional area as respective first holes in the remaining plurality of unfired ceramic plates such that the first holes define a cylinder of constant cross-sectional area throughout the entire thickness of the intermediate laminated structure, which is formed by the recited process steps. Specifically, the process steps recited in claim 9 include, among other things, a step of forming at least a first hole in a first unfired ceramic plate with a punch and pulling up the first unfired ceramic plate by closely attaching the first unfired ceramic plate to a stripper while leaving the punch in the first hole, forming at least a first hole in the second unfired ceramic plate with the punch and pulling up the second unfired ceramic plate together with the first unfired ceramic plate while leaving the punch in the second hole, forming first holes in the remaining unfired ceramic plates and sequentially stacking the punched, unfired ceramic plates along the punch as a stacking axis.

Independent claim 15 is a product-by-process claim for an intermediate laminated circuit substrate including, among other things, at least one cylinder defined by a plurality of first holes formed in each of a plurality of insulators and conductors by a punching operating and passing through all of the insulators and conductors, wherein at least a first hole in one of the plurality of insulators and conductors has the same shape and cross-sectional area as respective first holes in the remaining plurality of insulators and conductors such that the cylinder has a constant cross-sectional area

throughout the entire thickness of the intermediate laminated circuit substrate, which is formed by the recited process steps. Specifically, the process steps recited in claim 15 include, among other things, providing a plurality of wiring boards, forming at least a first hole in a first wiring board with a punch and pulling up the first wiring board by closely attaching the first wiring board to the stripper while leaving the punch in the first hole of the first wiring board, forming at least a first hole in a second wiring board with the punch and pulling up the second wiring board together with the first wiring board while leaving the punch in the first hole of the second wiring board, and forming first holes in the remaining wiring boards and sequentially stacking the punched wiring boards along the punch as a stacking axis.

Applicants respectfully submit that the process steps of claims 9 and 15 provide the respectively recited intermediate laminated structure and intermediate laminated circuit substrate, which are patentable over the applied references for the reasons explained above in connection with independent claims 1 and 11. Moreover, there is simply no disclosure or suggestion in the applied references of the specific process steps recited in independent claims 9 and 15, of any other steps performed to precisely align the respective holes in each green layer of the laminated structure, or even of any need for such precision alignment.

For at least the foregoing reasons, Applicants respectfully submit that claims 1-7 and 9-15 define patentable subject matter over the applied references. Accordingly, Applicants respectfully request that the above rejections be reconsidered and withdrawn.

Applicants respectfully request that the PTO acknowledge receipt and consideration of the references cited in the Information Disclosure Statement filed on October 6, 2004.

If Examiner Ha believes that contact with Applicants' attorney would be advantageous toward the disposition of this case, he is herein requested to call Applicants' attorney at the phone number noted below.

The Commissioner is hereby authorized to charge any additional fees associated with this communication or credit any overpayment to Deposit Account No. 50-1446.

Respectfully submitted,

November 3, 2004
Date

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